IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently amended) ~~Shared~~ A shared memory data transfer apparatus where a plurality of masters access one shared memory to perform data transfers, said shared memory data transfer apparatus comprising:

a plurality of master ~~interfaces~~ interface circuits respectively connected to the masters ~~master interfaces~~,

a plurality of write buffers ~~butters~~ respectively connected to the master ~~interfaces~~ interface circuits for retaining data written from said masters to said shared memory,

a plurality of read buffers ~~butters~~ respectively connected to the master ~~interfaces~~ interface circuits for retaining data read from said shared memory to said masters,

a FIFO coupled to said plurality of master interface circuits, and operable for receiving commands from said master interface circuits and ~~provided between said master interfaces and said shared memory~~ for storing commands ~~from the masters directed to said shared memory~~ in a first-in, first-out manner ~~fashion~~, and

a shared memory interface circuit coupled to said FIFO, said shared memory interface circuit operable for controlling data transfers from said write buffers to said shared memory or data transfers from said shared memory to said read buffers in accordance with commands fetched from said FIFO.

2. (Currently amended) ~~Shared~~ A shared memory access apparatus according to claim 1, comprising an arbiter for storing a plurality of simultaneously issued commands into said FIFO in a predetermined order.

3. (Currently amended) ~~Shared~~ A shared memory access apparatus according to claim 1 ~~or 2~~, comprising an arbiter for referencing the command contents and rearranging the order of commands to be stored into said FIFO.

4. (Currently amended) ~~Shared~~ A shared memory data transfer apparatus according to claim 1 ~~any one of claims 1 through 3~~, which issues commands to be stored into said FIFO per access to said shared memory.

5. (Currently amended) ~~Shared~~ A shared memory data transfer apparatus according to claim 1 ~~any one of claims 1 through 4~~, which uses a fixed burst length in an access to said shared memory.

6. (New) A shared memory data transfer apparatus according to claim 2, which issues commands to be stored into said FIFO per access to said shared memory.

7. (New) A shared memory data transfer apparatus according to claim 3, which issues commands to be stored into said FIFO per access to said shared memory.

8. (New) A shared memory data transfer apparatus according to claim 2, which uses a fixed burst length in an access to said shared memory.

9. (New) A shared memory data transfer apparatus according to claim 3, which uses a fixed burst length in an access to said shared memory.

10. (New) A shared memory data transfer apparatus according to claim 4, which uses a fixed burst length in an access to said shared memory.